Functions of Trap and Interrupt

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Trap and Interrupt are signals generated by software and hardware respectively. They break down the normal execution of the program. A brief description of trap and interrupt is given below.

Trap:

A trap is a software-generated interrupt (signal) caused by an error. Trap is also referred to as software interrupt. Software triggers an interrupt by executing special operation called system call.

Usually, trap is triggered when a numeric value is divided by zero, or unknown I/O device is accessed, etc. A trap will occur at exactly the same point of the program, whenever a program runs.

Interrupt:

An interrupt is a hardware-generated signal. It is sent to the CPU by an external hardware device such as I/O device. The CPU has a wire called the interrupt request line. An external hardware device sends interrupt signals (or requests) to the CPU through this line.

Hardware may trigger an interrupt at any time by sending a signal to the CPU. So an interrupt is dependent on the relative timing between the interrupting device and the CPU. Suppose an I/O module is performing I/O operation. It sends an interrupt signal to the CPU when the I/O operation is completed.

When the CPU is interrupted, then it: Suspends its current activities (such as execution of program). It performs a state save (i.e. saves the current state of the program counter (PC). Similarly, other state information is also saved). In many computer systems, this information is stored in a special Program Status Word (PSW) register. It transfers the control to the interrupt service routine. The interrupt service routine is executed; on completion, the CPU resumes the interrupted program.

Thus the application program does not have to contain any special code to accommodate the interrupts. The CPU and the operating system are responsible for suspending the program and then resuming it after performing necessary interrupt processing.

Interrupts are the important part of computer architecture and operating system. Each machine has its own interrupt mechanism, but most of the functions are common. When an interrupt is occurred, the control must be transferred to the appropriate interrupt service routine. Similarly, interrupt must be handled quickly.

In a computer system, only a predefined interrupts can be occurred, so an array of pointer is used to store the addresses of interrupt routines. This array of pointer is called the interrupt vector. Each trap and interrupt is associated with an index into that vector. The index values are the unique device numbers that provide the address of the interrupt service routine for interrupting device. The interrupt service routine is generally accessed through an interrupt vector.

The earlier computer systems stored the interrupt address in a fixed location or in a location indexed by the device number. However, modern computers use the stack for this purpose.

Classes of Interrupts:

There are many classes of interrupts, but the most common classes of interrupts are:

1. Program Check Interrupts:

Program Check Interrupts are caused by different problems during program execution. These problems may include division by zero, arithmetic overflow or underflow, incorrect format of input data etc. Many systems allow users, to specify their own routines to be executed when a Program Check Interrupt occurs.

2. Supervisor Call Interrupts:

Supervisor Call Interrupt is initiated by a running process that executes the supervisor call instruction. This type of interrupt is a user's request for a particular system service such as for performing I/O operation etc.

3. Timer Interrupts:

Timer interrupt is generated by timer within the CPU. Timer interrupt allows the operating system to perform certain functions on regular intervals of time.

4. I/O Interrupts:

I/O interrupts are generated by I/O controller (or I/O hardware). The I/O controller sends signal to the CPU that the status of device has changed I/O interrupts are caused when an I/O operation completes, an I/O error occurs, an I/O device gets ready etc.

5. External Interrupts:

These interrupts are caused by pressing the interrupt key by the operator, or receipt of a signal from another processor on a multiprocessor system.

6. Machine Check Interrupts:

These interrupts are caused by failure of any hardware component.

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